In the Claims:

Claims 1-15 (canceled).

Claim 16 (currently amended): An interconnect comprising:

(a) one or more metal lines formed from a first metal layer, said metal lines having gaps therebetween;

(b) low-k material filling all of the gaps between the metal lines and having ~~a height and one or more~~ at least one vertical portion~~s~~, said at least one vertical portion of said low-k material extending above said metal lines;

(c) a protective layer formed directly over and in direct contact with the metal lines and the low-k material, wherein the protective layer covers said at least one vertical portion of the low-k material;

(d) a dielectric layer formed over the protective layer, wherein the dielectric layer has a different composition than the low-k material and the protective layer;

(e) one or more vias etched in the dielectric layer;

(f) a metal for filling the vias;

(g) a second metal layer formed over the dielectric layer; and

(h) one or more openings in the protective layer for allowing the metal vias to contact the first metal lines.

Claim 17 (original): The interconnect of claim 16, wherein the protective layer includes an oxide.

Claim 18 (original): The interconnect of claim 17, wherein the oxide includes silicon dioxide.

Claim 19 (original): The interconnect of claim 16, wherein the protective layer includes a dielectric material.

Claim 20 (original): The interconnect of claim 19, wherein the protective layer includes silicon nitride.

Claim 21 (previously presented): The interconnect of claim 16, wherein the protective layer includes silicon carbide.

Claim 22 (currently amended): The interconnect of claim 16, further comprising a spacer disposed on ~~the~~said at least one vertical portion of the low-k material ~~in the vias~~.

Claim 23 (original): The interconnect of claim 16, wherein the protective layer is silicon-nitride.

Claim 24 (original): The interconnect of claim 16, wherein the first metal layer is an aluminum alloy, the metal filling the vias is tungsten, and the second metal layer is an aluminum alloy.

Claim 25 (original): The interconnect of claim 16, wherein the first metal layer is an aluminum alloy, the metal filling the vias is an aluminum alloy, and the second metal layer is an aluminum alloy.

Claim 26 (original): The interconnect of claim 16, wherein the dielectric layer is made of silicon dioxide, the protective layer is silicon nitride, and the low-k material is an organic low-k material.

Claim 27 (original): The interconnect of claim 16, wherein the dielectric layer is made of silicon dioxide, the protective layer is silicon nitride, and the low-k material is a porous silicon dioxide.

Claim 28 (previously presented): An interconnect structure comprising:

a plurality of metal lines formed on a substrate;

low-k dielectric structures interposed between two or more of said metal lines;

a second dielectric material formed above said metal lines, wherein portions of said second dielectric material are formed between portions of said low-k dielectric structures;

a protective layer interposed between said low-k dielectric structures and said second dielectric material, wherein said protective layer is configured to provide etch selectivity between said protective layer and said second dielectric material; and

a conductive feature formed within said second dielectric material and said protective layer, said conductive feature in contact with at least one of said plurality of metal lines.

Claim 29 (previously presented): The interconnect structure according to claim 28, wherein said protective layer includes dielectric material.

Claim 30 (previously presented): The interconnect structure according to claim 28, further comprising a liner disposed within a feature formed within said second dielectric material.

Claim 31 (previously presented): The interconnect structure according to claim 30, wherein said liner comprises a material selected from the group consisting of titanium, titanium nitride, tantalum, tantalum nitride, aluminum, copper, and tungsten nitride.

Claim 32 (previously presented): The interconnect structure according to claim 28, further comprising a spacer interposed between said low-k material and said conductive feature.

Claim 33 (previously presented): The interconnect structure according to claim 28, further comprising a spacer interposed between said low-k material and a liner.

Claim 34 (currently amended): An interconnect comprising:

(a) a plurality of metal lines formed from a first metal layer, said metal lines having gaps therebetween;

(b) material filling all of the gaps between the metal lines and having ~~a height and one or more~~ at least one vertical portion~~s~~, said at least one vertical portion of said material extending above said metal lines;

(c) a protective layer formed directly over and in direct contact with the metal lines and the material, wherein the protective layer covers said at least one vertical portion of the material;

(d) a dielectric layer formed over the protective layer, wherein the dielectric layer has a different composition than the protective layer;

(e) one or more vias etched in the dielectric layer;

(f) a metal within the vias;

(g) a second metal layer formed over and in direct contact with the dielectric layer; and

(h) one or more openings in the protective layer for allowing the metal in the vias to contact the metal lines.

Claim 35 (currently amended): An interconnect comprising:

(a) one or more metal lines formed from a first metal layer, said metal lines having gaps therebetween;

(b) low-k material filling all of the gaps between the metal lines and having ~~a height and one or more~~ at least one vertical portion~~s~~, said at least one vertical portion of said low-k material extending above said metal lines;

(c) a protective layer formed directly over the metal lines and the low-k material, wherein the protective layer covers said at least one vertical portion of the low-k material, and wherein the protective layer includes an oxide;

(d) a dielectric layer formed over the protective layer, wherein the dielectric layer has a different composition than the low-k material and the protective layer;

(e) one or more vias etched in the dielectric layer;

(f) a metal for filling the vias;

(g) a second metal layer formed over the dielectric layer; and

(h) one or more openings in the protective layer for allowing the metal vias to contact the first metal lines.

Claim 36 (previously presented): The interconnect of claim 35, wherein the oxide includes silicon dioxide.